EAST Search History

Ref #	Hits	Search Query	DBs	Default Operator	Plurals	Time Stamp
L1	25509303	@ad<"20040112"	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2007/11/09 17:42
L2	65	(RAM DRAM DDRAM "system memory") same tag near2 (buffer queue) and control with signal same (controller "control logic") and L1	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2007/11/09 17:42
L3	1	"4683555".PN.	USPAT; USOCR	OR	ON	2007/11/09 17:42
L4	2	"4796232".pn.	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2007/11/09 17:42
L5	1	"6810475".PN.	USPAT; USOCR	OR	ON	2007/11/09 17:42
L6	904	(bidirectional bi-directional) with buffer with controller	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2007/11/09 17:42
L7	4097	(bidirectional bi-directional) adj data adj bus	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2007/11/09 17:42
L8	1362	((RAM DRAM DDRAM) with buffer) and (memory adj controller) and (control adj logic)	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2007/11/09 17:42

EAST Search History

L9	54	L8 and L7 and @ad<"20040112"	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2007/11/09 17:42
L10	25509303	@ad<"20040112"	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2007/11/09 17:42
L11	836	interfac$3 with buffer with read$3 with writ$3 with memory with controller	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2007/11/09 17:42
L12	270	(bidirectional bi-directional) with bus with buffer with controller	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2007/11/09 17:42
L13	7	L12 and L10 and L11	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2007/11/09 17:42
L14	1734	711/100.ccls.	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2007/11/09 17:42
L15	8	(RAM DRAM DDRAM "system memory") same tag near2 (buffer queue) same read$3 same writ$3 and control with signal same (controller "control logic") and L1	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2007/11/09 17:42

EAST Search History

L16	2298	711/118.ccls.	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2007/11/09 17:42
L17	118	L12 same memory and L10	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2007/11/09 17:42
L18	431	buffer with logic$2 with decod$3 with controller	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2007/11/09 17:42
L19	10	(RAM DRAM DDRAM "system memory") same "read queue" same "write queue" same tag and L1	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2007/11/09 17:42
L20	1051	(RAM DRAM DDRAM "system memory") same read near2 (buffer queue) same write near2 (buffer queue) and L1	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2007/11/09 17:42
L21	2	"tag buffer" same (RAM DRAM DDRAM "system memory") same control near2 signal	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2007/11/09 17:42
L22	1	L1 and L21	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2007/11/09 17:42
L23	351	briggs.in.	US-PGPUB	OR	ON	2007/11/09 17:42

EAST Search History

L24	1	L23 and "tag buffer".clm.	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2007/11/09 17:42
L25	2	L23 and "bidirectional".clm.	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2007/11/09 17:42
L26	2	"read queue" same "write queue" same buffer with tag and L1	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2007/11/09 17:42
L27	18	L12 and L10 and L18	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2007/11/09 17:42
L28	1	"6754772".PN.	USPAT; USOCR	OR	ON	2007/11/09 17:42
L29	1	"20030005263".PN.	US-PGPUB	OR	ON	2007/11/09 17:42
L30	21	(RAM DRAM DDRAM) same "tag buffer" same controller and L1	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2007/11/09 17:42
L31	1265	711/105.ccls.	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2007/11/09 17:42

EAST Search History

L32	96	(RAM DRAM DDRAM) same buffer with tag same controller and L1	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2007/11/09 17:42
L33	293	711/101.ccls.	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2007/11/09 17:42
L34	28	L12 same memory same read$3 with writ$3 and L10	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2007/11/09 17:42
L35	25	(RAM DRAM DDRAM) same tag adj (buffer queue) same controller and L1	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2007/11/09 17:42
L36	1	"20030158992".PN.	US-PGPUB	OR	ON	2007/11/09 17:42
L37	1	"6400684".PN.	USPAT; USOCR	OR	ON	2007/11/09 17:42
L38	487	711/117.ccls.	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2007/11/09 17:42
L39	702	711/104.ccls.	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2007/11/09 17:42

EAST Search History

L40	3473	365/189.05.ccls.	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2007/11/09 17:43
L41	3632	365/189.01.ccls.	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2007/11/09 17:43
L42	10	(L16 L38 L31 L39 L41 L40 L14 L33) and L12 and L10	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2007/11/09 17:43
L43	2	"20050154820".pn.	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2007/11/09 17:43
L44	45	(RAM DRAM DDRAM "system memory") same tag near2 (buffer queue) same controller and L1	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2007/11/09 17:43
L45	1362	((RAM DRAM DDRAM) with buffer) and (memory adj controller) and (control adj logic)	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2007/11/09 17:43
L46	9	(RAM DRAM DDRAM "system memory") same tag near2 (buffer queue) same control with signal and L1	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2007/11/09 17:43

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L47	4	(RAM DRAM DDRAM "system memory") same tag near2 (buffer queue) same control with signal same controller and L1	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2007/11/09 17:43
L48	22	(L16 L38 L31 L39 L41 L40 L14 L33) and L6 and L10	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2007/11/09 17:43
L49	4	(RAM DRAM DDRAM "system memory") same "read queue" same "write queue" same buffer and L1	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2007/11/09 17:43
L50	48	read near2 (queue pipeline buffer) same write near2 (queue pipeline buffer) same tag near2 (queue pipeline buffer) and L1	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2007/11/09 17:43
L51	1	read near2 queue same write near2 queue same buffer same tag near2 queue and L1	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2007/11/09 17:43
L52	1718478	controller	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2007/11/09 17:43
L53	1781380	(buffer cache register)	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2007/11/09 17:43

EAST Search History

L54	2	"6363444".pn.	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2007/11/09 17:43
L55	25509303	@ad<"20040112"	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2007/11/09 17:43
L56	6673	L55 and (buffer cache) near5 controller near5 (BIU bus$3)	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2007/11/09 17:43
L57	925794	(bus$2 BIU)	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2007/11/09 17:43
L58	2298	711/118.ccls.	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2007/11/09 17:43
L59	222	L56 and L58	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2007/11/09 17:43
L60	50	L55 and tag adj2 (buffer cache queue) same controller same (RAM (system adj memory)) and tag near3 interface	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2007/11/09 17:43

EAST Search History

L61	34	L55 and tag adj2 (buffer cache queue) with controller and tag near3 interface	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2007/11/09 17:43
L62	14	L55 and tag near2 (buffer queue) with controller and tag near3 interface	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2007/11/09 17:43
L63	15	L55 and (buffer cache) with ((system adj memory) RAM) with controller same BIU	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2007/11/09 17:43
L64	6	L55 and (buffer cache) with BIU with bus with ((system adj memory) RAM) with controller	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2007/11/09 17:43
L65	2	"6546464".pn.	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2007/11/09 17:43
L66	523	"tag buffer"	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2007/11/09 17:43
L67	0	L55 and L66 with controller same (RAM (system adj memory)) and tag near3 interface	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2007/11/09 17:43

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L68	1	L55 and L66 same controller same (RAM (system adj memory)) and tag near3 interface	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2007/11/09 17:43
L69	0	L55 and L66 with controller with (RAM (system adj memory)) and tag near3 interface near3 control	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2007/11/09 17:43
L70	7	L55 and tag adj2 (buffer cache) with controller with (RAM (system adj memory)) and tag near3 interface	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2007/11/09 17:43
L71	0	L55 and L66 with controller with (RAM (system adj memory)) and tag near3 interface near3 control near3 bus	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2007/11/09 17:43
L72	17	L55 and tag adj2 (buffer queue) same controller and tag near3 interfac$3	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2007/11/09 17:43
L73	2	L55 and tag adj2 (buffer queue) same controller same bus$3 same (memory RAM) and tag near3 interface	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2007/11/09 17:43
L74	2	("2001/0052060").URPN.	USPAT	OR	ON	2007/11/09 17:43
L75	1	L55 and L74	USPAT	OR	ON	2007/11/09 17:43
L76	4	L55 and tag adj2 (buffer queue) same controller same bus$3 and tag near3 interfac$3	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2007/11/09 17:43

EAST Search History

L77	15597	L55 and (buffer cache) with controller with (BIU bus$3)	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2007/11/09 17:43

Terms used:
controller bidirectional bus tag buffer read write queue interleaved

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1 A survey of commercial parallel processors

Edward Gehringer, Janne Abullarade, Michael H. Gulyn

September 1988 **ACM SIGARCH Computer Architecture News**, Volume 16 Issue 4

Publisher: ACM Press

Full text available: pdf(2.96 MB) Additional Information: full citation, abstract, citings, index terms

This paper compares eight commercial parallel processors along several dimensions. The processors include four shared-bus multiprocessors (the Encore Multimax, the Sequent Balance system, the Alliant FX series, and the ELXSI System 6400) and four network multiprocessors (the BBN Butterfly, the NCUBE, the Intel iPSC/2, and the FPS T Series). The paper contrasts the computers from the standpoint of interconnection structures, memory configurations, and interprocessor communication. Also, the share ...

2 The sun fireplane system interconnect

Alan Charlesworth

November 2001 **Proceedings of the 2001 ACM/IEEE conference on Supercomputing (CDROM) Supercomputing '01**

Publisher: ACM Press

Full text available: pdf(224.87 KB) Additional Information: full citation, abstract, references, citings, index terms

System interconnect is a key determiner of the cost, performance, and reliability of large cache-coherent, shared-memory multiprocessors. Interconnect implementations have to accommodate ever greater numbers of ever faster processors. This paper describes the Sun™ Fireplane two-level cache-coherency protocol, and its use in the medium and large-sized UltraSPARC-III-based Sun Fire™ servers.

3 The Alpha demonstration unit: a high-performance multiprocessor

Charles P. Thacker, David G. Conroy, Lawrence C. Stewart

February 1993 **Communications of the ACM**, Volume 36 Issue 2

Publisher: ACM Press

Full text available: pdf(6.26 MB) Additional Information: full citation, references, citings, index terms, review

Keywords: Alpha AXP chip

4 A VLIW architecture for a trace scheduling compiler

Robert P. Colwell, Robert P. Nix, John J. O'Donnell, David B. Papworth, Paul K. Rodman
October 1987 **ACM SIGARCH Computer Architecture News , ACM SIGPLAN Notices , ACM SIGOPS Operating Systems Review , Proceedings of the second international conference on Architectual support for programming languages and operating systems ASPLOS-II**, Volume 15 , 22 , 21 Issue 5 , 10 , 4
Publisher: IEEE Computer Society Press, ACM Press

Full text available: pdf(1.59 MB) Additional Information: full citation, abstract, references, citings, index terms

Very Long Instruction Word (VLIW) architectures were promised to deliver far more than the factor of two or three that current architectures achieve from overlapped execution. Using a new type of compiler which compacts ordinary sequential code into long instruction words, a VLIW machine was expected to provide from ten to thirty times the performance of a more conventional machine built of the same implementation technology.Multiflow Computer, Inc., has now built a VLIW called the TRACE™< ...

5 GI-cube: an architecture for volumetric global illumination and rendering

Frank Dachille, Arie Kaufman
August 2000 **Proceedings of the ACM SIGGRAPH/EUROGRAPHICS workshop on Graphics hardware HWWS '00**
Publisher: ACM Press

Full text available: pdf(650.91 KB) Additional Information: full citation, abstract, references, citings, index terms

The power and utility of volume rendering is increased by global illumination. We present a hardware architecture, GI-Cube, designed to accelerate volume rendering, empower volumetric global illumination, and enable a host of ray-based volumetric processing. The algorithm reorders ray processing based on a partitioning of the volume. A cache enables efficient processing of coherent rays within a hardware pipeline. We study the flexibility and performance of this new architecture using both ...

Keywords: hardware accelerator, volume processing, volume rendering, volumetric global illumination, volumetric ray tracing

6 Coherence Ordering for Ring-based Chip Multiprocessors

Michael R. Marty, Mark D. Hill
December 2006 **Proceedings of the 39th Annual IEEE/ACM International Symposium on Microarchitecture MICRO 39**
Publisher: IEEE Computer Society
Full text available: pdf(220.54 KB) Additional Information: full citation, abstract, index terms

Ring interconnects may be an attractive solution for future chip multiprocessors because they can enable faster links than buses and simpler switches than arbitrary switched interconnects. Moreover, a ring naturally orders requests sufficiently to enable directory-less coherence, but not in the total order that buses provide for snooping coherence. Existing cache coherence protocols for rings either establish a (total) ordering point (ORDERING-POINT) or use a greedy order (GREEDY-ORDER) with unb ...

7 A survey of processors with explicit multithreading

Theo Ungerer, Borut Robič, Jurij Šilc
March 2003 **ACM Computing Surveys (CSUR)**, Volume 35 Issue 1
Publisher: ACM Press

Full text available: pdf(920.16 KB) Additional Information: full citation, abstract, references, citings, index terms

Hardware multithreading is becoming a generally applied technique in the next generation of microprocessors. Several multithreaded processors are announced by industry or already into production in the areas of high-performance microprocessors, media, and network processors.A multithreaded processor is able to pursue two or more threads of control in parallel within the processor pipeline. The contexts of two or more threads of control are often stored in separate on-chip register sets. Unused i ...

Keywords: Blocked multithreading, interleaved multithreading, simultaneous multithreading

8 Paradigms for process interaction in distributed programs

Gregory R. Andrews
March 1991 **ACM Computing Surveys (CSUR)**, Volume 23 Issue 1
Publisher: ACM Press

Full text available: pdf(3.77 MB) Additional Information: full citation, abstract, references, citings, index terms, review

Distributed computations are concurrent programs in which processes communicate by message passing. Such programs typically execute on network architectures such as networks of workstations or distributed memory parallel machines (i.e., multicomputers such as hypercubes). Several paradigms—examples or models—for process interaction in distributed computations are described. These include networks of filters, clients, and servers, heartbeat algorithms, probe/echo algorithms, broa ...

Keywords: clients and servers, distributed and parallel algorithms, distributed programming, distributed programming methods, heartbeat algorithms, networks of filters, patterns for interprocess communication, probe/echo algorithms, replicated servers, token-passing algorithms

9 Evaluation of architectural support for global address-based communication in large-scale parallel machines

Arvind Krishnamurthy, Klaus E. Schauser, Chris J. Scheiman, Randolph Y. Wang, David E. Culler, Katherine Yelick
October 1996 **ACM SIGOPS Operating Systems Review , ACM SIGPLAN Notices , Proceedings of the seventh international conference on Architectural support for programming languages and operating systems ASPLOS-VII**, Volume 30 , 31 Issue 5 , 9
Publisher: ACM Press

Full text available: pdf(1.42 MB) Additional Information: full citation, abstract, references, citings, index terms

Large-scale parallel machines are incorporating increasingly sophisticated architectural support for user-level messaging and global memory access. We provide a systematic evaluation of a broad spectrum of current design alternatives based on our implementations of a global address language on the Thinking Machines CM-5, Intel Paragon, Meiko CS-2, Cray T3D, and Berkeley NOW. This evaluation includes a range of compilation strategies that make varying use of the network processor; each is optimiz ...

10 Leveraging Optical Technology in Future Bus-based Chip Multiprocessors

Nevin Kirman, Meyrem Kirman, Rajeev K. Dokania, Jose F. Martinez, Alyssa B. Apsel, Matthew A. Watkins, David H. Albonesi
December 2006 **Proceedings of the 39th Annual IEEE/ACM International Symposium on Microarchitecture MICRO 39**
Publisher: IEEE Computer Society

Full text available: pdf(589.69 KB) Additional Information: full citation, abstract, index terms

Although silicon optical technology is still in its formative stages, and the more near-term application is chip-to-chip communication, rapid advances have been made in the development of on-chip optical interconnects. In this paper, we investigate the integration of CMOS-compatible optical technology to on-chip cache-coherent buses in future CMPs. While not exhaustive, our investigation yields a hierarchical opto-electrical system that exploits the advantages of optical technology while abiding ...

11 The SAGE graphics architecture

Michael Deering, David Naegle

July 2002 **ACM Transactions on Graphics (TOG) , Proceedings of the 29th annual conference on Computer graphics and interactive techniques SIGGRAPH '02**, Volume 21 Issue 3

Publisher: ACM Press

Full text available: pdf(17.26 MB) Additional Information: full citation, abstract, references, citings, index terms

The Scalable, Advanced Graphics Environment (SAGE) is a new high-end, multi-chip rendering architecture. Each single SAGE board can render in excess of 80 million fully lit, textured, anti-aliased triangles per second. SAGE brings high quality antialiasing filters to video rate hardware for the first time. To achieve this, the concept of a frame buffer is replaced by a fully double-buffered sample buffer of between 1 and 16 non-uniformly placed samples per final output pixel. The video output ra ...

Keywords: anti-aliasing, frame buffer algorithms, graphics hardware, graphics systems, hardware systems, rendering hardware, video

12 Distributed systems - programming and management: On remote procedure call

Patrícia Gomes Soares

November 1992 **Proceedings of the 1992 conference of the Centre for Advanced Studies on Collaborative research - Volume 2 CASCON '92**

Publisher: IBM Press

Full text available: pdf(4.52 MB) Additional Information: full citation, abstract, references, citings

The Remote Procedure Call (RPC) paradigm is reviewed. The concept is described, along with the backbone structure of the mechanisms that support it. An overview of works in supporting these mechanisms is discussed. Extensions to the paradigm that have been proposed to enlarge its suitability, are studied. The main contributions of this paper are a standard view and classification of RPC mechanisms according to different perspectives, and a snapshot of the paradigm in use today and of goals for t ...

13 An adaptive, non-uniform cache structure for wire-delay dominated on-chip caches

Changkyu Kim, Doug Burger, Stephen W. Keckler

October 2002 **ACM SIGPLAN Notices , ACM SIGARCH Computer Architecture News , ACM SIGOPS Operating Systems Review , Proceedings of the 10th international conference on Architectural support for programming languages and operating systems ASPLOS-X**, Volume 37 , 30 , 36 Issue 10 , 5 , 5

Publisher: ACM Press

Full text available: pdf(1.33 MB) Additional Information: full citation, abstract, references, citings

Growing wire delays will force substantive changes in the designs of large caches. Traditional cache architectures assume that each level in the cache hierarchy has a single, uniform access time. Increases in on-chip communication delays will make the hit time of large on-chip caches a function of a line's physical location within the cache. Consequently, cache access times will become a continuum of latencies rather than a single discrete latency. This non-uniformity can be exploited to provide ...

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